Failure Analysis Terms and Definitions

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Acceptor n: in a semiconductor, an impurity in a semiconductor that accepts electrons excited from the valence band, leading to hole conduction. [SEMI M1-94 and ASTM F1241] Also see hole

Access time n : a time interval that is characteristic of a storage device and is essentially a measure of time required to communicate with that device. [IEEE]

Acoustic Micro Imaging (AMI) : A method of evaluating materials and bonding for various microelectronic application by using high frequency ultrasound from 5-300 MHz to image the internal features of the samples. [ISTFA]

Accumulation condition n: the region of the capacitance-voltage (C-V) curve for which a 5-V increment toward a more negative voltage for p-type material, or toward a more positive voltage for n-type material, results in a change of less than 1% in the maximum capacitance, Cmax. [ASTM F1241]

Active area n : the region of thin oxide on a die or wafer in which transistors and other circuits reside. [SEMATECH]

Active devices n: semiconductor devices that have active function, such as integrated circuits and transistors. [SEMI G35-87] Contrast passive devices.

Adhesion, resist edge n : the ability of the edge of an image in a development resist coating to adhere to its substrate under applied physical or chemical stress. [ASTM F127-84]

Adhesive stringer n : on a photolithographic pellicle, any detectable protrusion from the edge of the adhesive. [SEMI p5-94]

Aeolotropic : see anisotropic

AES : see Auger electron spectroscopy

AFM : see Atomic Force Microscopy

Alignment n 1: the accuracy of the relative position of an image on a reticle with reference to an existing image on a substrate [SEMATECH] 2 : a procedure in which a wafer is correctly positioned relative to a reticle. [SEMATECH] 3 : the mechanical positioning of reference points on a wafer or flat panel display substrate (also called alignment marks or

alignment targets) to the corresponding points on the reticle or reticles. The measure of alignment is the overlay at the positions on the wafer or substrate where the alignment marks are placed. [Adapted from SEMI P18-92 and D8-94] Also see direct alignment and indirect alignment.

Alloy n 1: a composite of two or more elements, of which at least one is metal. [SEMATECH] 2 : a thermal cycle in which two or more discrete layers (of which at least one is metal) react to allow good electrical contacts. [SEMATECH}

Aluminized area n : in a cerdip or cerpack semiconductor package, the lead frame area coated with aluminum to provide a surface suitable for wire bonding. The maximum area is defined by the inside dimension of the cap or ceramic ring. In some cases, the die attach area is also coated if a full lead frame is used. The coating may be vacuum deposited or bonded. [SEMATECH]

Aluminized width n : in a semiconductor package, the width of the area coated with a protective layer of aluminum. This area covers most of the top formed width. [SEMATECH] Also see package, bond finger, top formed width, and aluminized area.

Aluminum (Al) n : a metal used to interconnect the devices on a wafer and to interconnect external devices or components. [SEMATECH]

Ambient temperature (TA) 1: the temperature of the surrounding medium, such as air or liquid, that comes into contact with the device or apparatus. [SEMATECH} 2: the temperature of the specified , surrounding medium (such as air, nitrogen, or a liquid) that comes into contact with a semiconductor device being tested for thermal resistance. [SEMI G38-87]

AMI : See Acoustic Micro Imaging

Ammonium fluoride (NH_4F) : a white crystalline salt used to buffer hydrofluoric acid etches that dissolve silicon dioxide by not silicon. An example of such an etch is the buffered oxide etch. [SEMATECH] Also see pinhole.

Ammonium hydroxide (NH_4OH) : a weak base formed when ammonia is dissolved in water. [SEMATECH]

Amorphous silicon : silicon with no discernible crystalline structure. [SEMATECH] Contrast polycrystalline silicon.

Analog adj : A signal in an electronic circuit that takes on a continuous range of values rather than only a few discrete values; a circuit or system that processes analog signals. [1994 National Technology Roadmap for Semiconductors] Contrast discrete

Angle-resolved scattering (ARS) n : technique that measures light scattered from particles as a function of angle; used to characterize particles. [SEMATECH]

Angstrom (Å) n : unit of linear measure equal to one ten billionths of a meter (10^{-10} m). The diameter of a human hair is approximately 750,000 Å.) The preferred SI unit is nanometers. 10 Å = 1 nm. [SEMATECH]

Anion n: an ion that is negatively charged. [SEMATECH]

Anisotropic adj. : exhibiting different physical properties in different directions. NOTE – In semiconductor technology, the different directions are defined by the crystallographic planes. [SEMI M1-94 and ASTM F1241] Also called non-isotropic and aeolotropic. Also see anisotropic etch

Anisotropic etch n: a selective etch that exhibits an accelerated etch rate along specific crystallographic planes. NOTE – Anisotropic etches are used to determine crystal orientation, to expose crystal defects, and to facilitate dielectric component isolation. [SEMI M1-94 and ASTM F1241] Also called preferential etch. Also see anisotropic.

Anneal n : a high-temperature operation that relieves stress in silicon, activates ion-implanted dopants, reduces structure defects and stress, and reduces interface charge at the silicon-silicon dioxide interface [SEMATECH]

Anomaly: see defect

Antireflective coating (ARC) n : a layer of dielectric material deposited on a wafer before resist to minimize reflections during resist exposure. [SEMATECH]

Antimony (Sb) n: a brittle, tin-white, metallic chemical element of crystalline structure. Antimony is used as an n-type dopant in silicon, often for the buried layer. [SEMATECH]

Avalanche photo-diode (APD): Solid-state detector with high quantum efficiency in the near infrared region. [ISTFA]

APD : See Avalanche photo-diode.

ARC : see antireflective coating.

Architecture n : of a computer system, a defined structure based on a set of design principles . The definition of the structure includes its components, their functions, and their relationships and interactions. [SEMATECH]

Area contamination n : foreign matter on localized portions of a wafer or substrate surface. [SEMI M3-88]

Arsenic (As) n: a highly poisonous chemical element, which is brittle and steel gray in color. Arsenic is often used as a n-type dopant for buried layer predisposition. [SEMATECH] Also see n-type.

Artifact n 1: a physical standard against which a parameter is measured; for example, a test wafer used for testing parametric drift in a machine. [SEMATECH] Also called

standard reference material. 2 : a superficial or unessential attribute of a process or characteristic under examination; for example, a piece of lint on a lens that appears through a microscope to be a defect on a die. [SEMATECH] 3 : in surface characterization, any contribution to an image from other than true surface morphology. Examples include contamination, vibration, electronic noise, and instrument imperfections. [SEMATECH]

Ash v : to apply heat to a material until the material has been reduced to a mineral residue [SEMATECH]

Asher n : a machine used to remove resist from substrates. [SEMATECH]

Ashing n : the operation of removing resist from a substrate by oxidation; a reaction of resist with oxygen to remove the resist from the substrate. [SEMATECH]

Aspect ratio n 1: in etch, the depth-to-width ratio of an opening of a wafer. 2 : in feature profile, the ratio of height to width of a feature. [SEMATECH]

Atomic force microscopy (AFM) n: a microscopy technique based on profilometry using an atomically sharp probe that provides three-dimensional highly magnified images. During AFM, the probe scans across a sample surface. The changes in force between the sample and the probe tip cause a deflection of the probe tip that is monitored and used to form the magnified image. [SEMATECH]

Atomic percent n: in electron spectroscopy for chemical analysis (ESCA) of plastic surface composition, the number of atoms of a particular element present in every hundred atoms within the ESCA detection volume. [SEMATECH]

ATPG : see automatic test pattern generation.

At-speed test n: any test performed on an integrated circuit that tests the device at its normal operating clock frequency. [1994 National Technology Roadmap for Semiconductors]

Auger electron spectroscopy (AES) n : the energy analysis of auger electrons produced when an excited atom relaxes by a radiationless process after ionization by a high-energy electron, ion, or X-ray beam [SEMATECH] Also called Atomic-emission spectroscopy, SAM, Scanning Auger microprobe

Auger process n: the radiationless relaxation of an atom involving a vacancy in an inner electron shell. An electron is emitted, which is referred as an Auger electron [ASTM E673-90]

Autodoping n : in the manufacture of silicon epitaxial wafers, the incorporation of dopant originating from the substrate into the expitaxial layer [SEMI M1-94 and ASTM F1241] Also called self-doping. Also see doping and substrate.

Automatic test pattern generation (ATPG) n : the automatic development of vectors which, when applied to an integrated circuit, permit faults to be detected in the performance of the integrated circuit. [1994 National Technology Roadmap for Semiconductors]

Back-end of line (BEOL) n : process steps from contact through completion of the wafer prior to electrical test. Also called back end. [SEMATECH]

Backgrind n : an operation using an abrasive on the back side of a substrate to achieve the necessary thinness for scribing, cutting, and packaging of die. [SEMATEC]

Back oxide n : a layer of silicon dioxide formed on the back of a wafer during oxidation. [SEMATECH]

Back surface n : of a semiconductor wafer, the exposed surface opposite to that on which active semiconductor devices have been or will be fabricated. [ASTM F1241] Also called backside.

Bake n: in wafer manufacturing, a process step in which a wafer is heated in order to harden resist, remove moisture, or cure a film deposited on the wafer. [SEMATECH]

Ball-grid array (BGA) n : an integrated circuit surface mount package with an area array of solder balls that are attached to the bottom side of a substrate with routing layers. The die is attached to the substrate using die and wire bonding or flip-chip interconnection. [SEMATECH] Also called land-grid array, pad-grid array, or pad-array carrier

Bar : see die, crossbar, and bar end.

Bare die n : individual, unpackaged silicon integrated circuits. [1994 National technology Roadmap for Semiconductors]

Barrier n : a physical layer designed to prevent intermixing of the layers above and below the barrier layer; for example, titanium tungsten and titanium-nitride layers. [SEMATECH]

Barrier layer : see depletion layer.

Base n 1 : in semiconductor manufacturing chemicals, a substance that dissociates in water to liberate hydroxyl ions, accepts a proton, has an unshared pair of electron, or reacts with acid to forma salt. A base ha a pH greater than 7 and turns litmus paper blue. [SEMATECH] 2 : in facilities and safety, a corrosive material with the chemical reaction characteristic of an electron donor. [SEMI S4-92] 3 : in quartz and high temperature carriers, the material at the bottom of a wafer carrier on which the wafer carrier rests when placed on a flat surface [SEMI E2-93] 4 : of a frame, a window frame, and the cap are attached to the base – generally with devitrifying solder glass – during package/device manufacture. [SEMI G1-85] Also see cap and window frame.

Behavioral n :a level of logic designed that involves describing a system at a level of abstraction that does not involve detailed circuit elements, but instead expresses the circuit functionality linguistically or as equations. [1994 National Technology Roadmap for Semiconductors]

BEOL : see back-end of line

BFM : see bit map fail.

BGA : see ball grid array.

BiCMOS design n : the combination of bipolar and complementary metal oxide semiconductor design and processing principles on a single wafer or substrate. [SEMATECH]

Bimetal mask : see mask, bi-metal.

Binding energy n : the value obtained by subtracting the instrumentally measured kinetic energy of an electron from the energy of the incident photon, corrected for an instrument work function. [SEMATECH]

Bipolar adj : a semiconductor device fabrication that produces transistors which use both holes and electrons as charge carriers. [SEMI M1-94 and ASTM F1241]

Bird's beak n : a structural feature produced as a result of the lifting of the edges of the nitride layer during subsequent oxidation. [SEMATECH]

BIST : see built-in self test.

Bit Fail Map : A matrix of 0s and 1s describing passing and failing SRAM cells at test. [ISTFA]

Blister ceramic n : an enclosed, localized separation within or between the layers of a ceramic package that does not expose an underlying layer of ceramic or metallization. [SEMI G61-94] Also called bubble ceramic.

Blister metal n : in packaging, an enclosed, localized separation of a metallization layer from its base material (such as ceramic or another metal layer) that does not expose the underlying layer. [SEMI G8-94] Also called bubble metal, blister metallization, and bubble metallization. Also see package.

BOAC : See copper bonding over active circuit.

Bonding pads n : relatively large metal areas on a die used for electrical contact with a package or prove pins. [SEMATECH]

Boundary scan n : a scan path that allows the input/output pads of an integrated circuit to be both controlled and observed. [1994 National Technology Roadmap for Semiconductors]

Bridge n 1: a defect in which two adjacent areas connect because of mis-processing such as poor lithography, particle contamination, underdevelop, or etch problems. [SEMATECH] Also called short. 2 : software that allows access to, and combination of, data from incompatible databases. [SEMATECH]

Bridging fault n : a fault modeled as a short-circuit between two nets on a die. [1994 National Technology Roadmap for Semiconductors]

Brightfield illumination n : (transmission electron microscopy) : the illumination of an object so that it appears on a bright background.

Buffered hydrofluoric acid n : an extremely hazardous corrosive used to etch silicon dioxide from a wafer. This aid has a 20- to 30-minute reaction delay after contact with skin or eyes. [SEMATECH]

Built-in self test (BIST) : any of the methods of testing an integrated circuit (IC) that uses special circuits designed into the IC. This circuitry then performs test functions on the IC and signals whether the parts of the IC covered by the BIST circuits are working properly. [1994 National Technology Roadmap for Semiconductors]

Buried contact n : a conductive region between two less conductive regions. [SEMATECH]

Buried layer n 1 : a conductive layer between two less conductive films; for example, a localized n+ region in a p-type wafer that reduces the npn collector series resistance for integrated circuit transistors fabricated in an n-type epitaxial layer deposited on the p-type wafer. [SEMATECH] 2: in epitaxial silicon wafers, a diffused region in a substrate that is, or is intended to be, covered with an epitaxial layer. [SEMI M18-94 and ASTM F1241] Also called subdiffused layer and diffusion under film.

Burn-in n : the process of exercising an integrated circuit at elevated voltage and temperature. This process accelerates failure normally seen as "infant mortality" in a chip. The resultant test product is of high quality. [1994 National Technology Roadmap for Semiconductors] Also see infant mortality.

C4 (controlled collapse chip connect) : see flip chip.

C-AFM : see conductive atomic force microscopy.

Cap deposition : see passivation.

Carrier n 1 : an entity capable of carrying electric charge through a solid; for example, mobile holes and condition electrons in semiconductors. [SEMI M1-94 and ASTM F1241] Also called charge carrier. Also see majority carrier and minority carrier. 2 : slang for wafer carrier. [SEMATECH]

Cavity-down packages n : in cofired ceramic packages, packages on which the die surface faces the mounting board. [SEMI G61-94]

Cavity-up packages n : in cofired ceramic packages, packages on which the die surface faces away from the mounting board. [SEMI G61-94]

Cerdip : abbreviation for ceramic dual-in-line package.

Channel : the portion of a MOS integrated circuit that allows current to flow when biased by the overlying gate region [Sandia Labs]

Chemical-mechanical polish (CMP) n : a process for the removal of surface material from a wafer. The process uses chemical and mechanical actions to achieve a mirror-like surface for subsequent processing. [SEMI M1-94 and ASTM F1241] Contrast physical vapor deposition.

Chem-mech polish : See chemical-mechanical polish.

Chip n 1 : in semiconductor wafers, a region where material has been unintentionally removed from the surface or edge of the wafer. [ASTM F1241] Contrast indent. 2 : see die. 3 : in packaging, a region of material missing from a component; for example, ceramic from a package or solder from a preform. The region does not process completely through the component and is formed after the component is manufactured. The chip size is given by its length, width, and depth from a projection of the design plan-form. [SEMI G61-94] Also called chip-out. Contrast pit. 4 : in flat panel display substrates, a region of material missing from the edge of the glass substrate, which is sometimes caused by breakage or handling. [SEMI D9-94]

Chip carrier (CC) n : a small footprint semiconductor package generally with terminals on all four sides. The package may be manufactured by cofired ceramic or multilayer printed circuit board technologies. [SEMATECH] Also see castellation and ceramic chip carrier

Chip-out : see chip.

Circuit n : the combination of a number of connected electrical elements or parts to accomplish a desired function. [SEMATECH]

Circuit design n : techniques used to connect active (transistors) and passive (resistors, capacitors, and inductors) elements in a manner to perform a function (that is, logic, analog). [1994 National Technology Roadmap for Semiconductors]

Circuit geometries n : the relative shapes and sizes of features on a die. [SEMATECH]

CMOS : see complementary metal oxide semiconductor.

CMP : see chemical-mechanical polish.

COA : see copper over anything

Comet n : on a substrate, a buildup of resist shaped like a comet and generated by a defect. [SEMI P3-90] Also called motorboat.

Complementary metal oxide semiconductor (CMOS) n: a fabrication process that incorporates p-channel and n-channel MOS transistors within the same silicon substrate. [SEMATECH]

Component n 1 : an individual electronic part, such as a device, diode, or capacitor that is fabricated in a metal oxide semiconductor or bipolar process. [SEMATECH] 2 : an individual piece or a complete assembly of individual pieces, including industrial products that are manufactured as independent units, capable of being joined with other pieces or components. The typical components referred to by the specification are valves, fittings, regulators, gauges, instrument sensors, a single length of tubing, several pieces of tubing welded together, tubing welded to fittings, and the like. [SEMI F1-90] 3 : the fundamental parts of an object, its entities, or relationships. [SEMATECH] 4 : the hardware and software that work in sets (functional entities) to perform the operation (s). [SEMATECH]

Conchoidal fracture n : a fracture having smooth convexities and concavities like a clamshell. [SEMATECH] Also see chip.

Conductive atomic force microscopy (C-AFM): An SPM technique that has been widely used for electrical characterization of dielectric film and gate oxide integrity. [ISTFA]

Conductor n : refers to a microscope design with superior abilities to image submicron features on a wafer. [1994 national Technology Roadmap for Semiconductors]

Contact n : in an oxide layer, an opening that allows electrical connection between metal and silicon layers. [SEMATECH] Also see window and via.

Contamination n 1 : the presence of particles, chemicals and other undesirable substances, such as on or in a process tool, in a process liquid or in a clean room environment. [SEMATECH] Also see area contamination and particulate contamination. 2 : three-dimensional foreign material adhering to a package)plastic or ceramic) or leadframe, or parent material displaced from its normal location and similarly adhered. Adherence means that the particle cannot be removed by an air or nitrogen blast at 20 psi. [SEMATECH] Also see foreign material and stain.

Controlled collapse chip connect (C4) : see flip chip

Copper bonding over active circuit: growing copper over any underlying aluminum metallization. Bonding is done on the top most copper layer. [ISTFA]

Copper over anything : having copper over anything but does not require copper on the top layer.

Correlation n 1 : a relation existing between phenomena or things or between mathematical or statistical variables which tend to vary, be associated, or occur together in a way not expected on the basis of chance alone. [Webster's Dictionary]

Crack n 1 : on semiconductor wafers, a cleavage or fracture that extends to the surface and may or may not pass through the entire thickness of the wafer. [ASTM F1241] 2 : of a semiconductor package or solder preform, a cleavage or fracture that extends to the surface. The crack may or may not pass through the entire thickness of the package or preform. [SEMI G61-94] 3 : in flat panel display substrates, a fissure located at the sheet edge or central area. [SEMI D9-94]

Crater n : on the surface of a slice or wafer, an individually distinguishable bowl-shaped cavity. A crater is visible when viewed under diffused illumination. [SEMATECH]

Cratering n : on a slice or wafer, a surface texture of irregular closed ridges with smooth central regions. [ASTM F1241]

Crescents n : structures with parallel major axes, attributed to substrate defects either above or below the surface plane of silicon substrates after epitaxial deposition. [ASTM F1241] Also see fishtails.

Critical area n : the area in which the center of a defect must occur to cause a failure or fault. [SEMATECH] Also see fault and fault probability.

Critical dimension (CD) n : the width of a patterned line or the distance between two lines, monitored to maintain device performance consistency; that dimension of a specified geometry that must be within design tolerances. [ASTM F127-84] Also see linewidth.

Crosstalk n: the undesirable addition of one signal to another in a circuit usually caused by coupling through parasitic elements. An example would be inductive or capacitive coupling between adjacent conductors. [1994 National Technology Roadmap for Semiconductors]

Crossunder n : on a die, the point at which a conductor crosses under a second conductor without making electrical contact. [SEMATECH]

Crow's foot n : on a semiconductor wafer, intersecting cracks in a pattern resembling a "crow's foot" Y on {111} surfaces and a cross "+" on {100} surfaces. [ASTM F1241]

Crystal n : a solid composed of atoms, ions, or molecules arranged in a pattern that is periodic in three dimensions. [ASTM F1241]

Crystal defect n : departure from the regular arrangement of atoms in the ideal crystal lattice. [ASTM F1241] Also see crystal lattice and damage.

Crystal indices : see Miller indices. Also see crystallographic notation.

Crystal lattice n : in a crystal, the three-dimensional and repeating pattern of atoms. [SEMATECH]

Crystallographic notation n : a symbolism based on Miller indices used to label planes and directions in a crystal as follows: (111) plan [111] direction {111} family of planes <111 family of directions. [SEMI M1-94 and ASTM F1241]

Crystal originated particle (COP) n : a surface depression that is formed during soft alkaline chemical treatment of silicon wafer surfaces that contain crystal defects at or close to the wafer surface and that scatters light similarly to a very small particle. [ASTM F1241] Also called surface micro defect.

CTE : see coefficient of thermal expansion.

CVD : see chemical vapor deposition.

Cycle time n : (1) the length of time required for a wafer to complete a specified process or set of processes. [SEMATECH] (2) the length of time required to complete a failure analysis job from receipt in the failure analysis lab to the time results (written or verbal) are communicated back to the immediate requestor. [Sandia Labs] Also see equipment cycle, minimum theoretical cycle time, and theoretical cycle time.

Damascene n : an integrated circuit process by which a metal conductor pattern is embedded in a dielectric film on the silicon substrate. The result is a planar interconnection layer. The creation of a damascene structure most often involves chemical mechanical polishing of a nonplanar surface resulting from multiple process steps. A damascene trench is a filled trench. [1994 National Technology Roadmap for Semiconductors]

Damage n 1 : of a single-crystal silicon specimen, a defect of the crystal lattice in the form of irreversible deformation that results from mechanical surface treatments such as sawing, lapping, grinding, sandblasting, and shot peening at room temperature without subsequent heat treatments. [ASTM F1241] Also see crystal lattice. 2 : any yield or reliability detractors other than those related to design, process specification violations, or particles. [SEMATECH]

DC test : A sequence of direct current (DC) measurements performed on integrated circuit pads to determine probe

contact, leakage currents, voltage levels on input and output, power supply currents, etc. [1994 national Technology Roadmap or Semiconductors]

Deep level impurity n : a chemical element that, when introduced into a semiconductor , has an energy level (or levels) that lies on the midrange of the forbidden energy gap, between the energy levels of the dopant impurity species. [ASTM F1241]

Defect n : for silicon crystals, a chemical or structural irregularity that degrades the ideal silicon crystal structure or the thin films built over the silicon wafer. 2 : a pit, tear, groove, inclusion, grain boundary, or other surface feature that is either characteristic of the material or a result of its processing and that is not a result of the sample preparation. [SEMATECH] Also called anomaly.

Defect density n : the number of imperfections per unit area, where imperfections are specified by type and dimension. [ASTM F127-84] Also see defect.

Defect level n : the number of die in parts-per-million that are shipped to customers and that are defective en though the test program declares them to be good. [1994 National technology Roadmap for Semiconductors]

Defect, photomask n : any flaw or imperfection in the opaque coating or functional pattern that will reproduce itself in a resist film to such a degree that it is pernicious to the proper functioning of the microelectronic device being fabricated. [SEMI P2-86]

Deformation n : a difference between the IC structure of the fabricated device and the desired structure of the nominal device. [ISTFA]

Deforming event : The deviation from nominal manufacturing conditions resulting in an IC deformation. [ISTFA]

Delamination n : in a cofired ceramic package, chip carrier, dual inline, pin grid array, etc., the separation of one ceramic layer from another . [SEMI G61-94] Also see package.

Delay fault n : a fault that has the effect of causing a signal to appear late in arriving at a destination. [1994 National Technology Roadmap for Semiconductors]

Design for test (DFT) n : design of logic circuits to facilitate electrical testing. [SEMATECH]

Destructive physical analysis n 1: the examination and testing of components to ensure proper operation and behavior. [Sandia labs]

Device n : a specific kind of electronic component (such as a MOS transistor, resistor, diode or capacitor) on a die. The diode and transistor are referred to as active devices the capacitor and resistor, as passive devices. [SEMATECH]

Dew point n : the temperature at which liquid first condenses when vapor is cooled. [SEMI C3-94]

DFT : see design for test.

Die n (sing or pl) : a small piece of silicon wafer, bounded by adjacent scribe lines in the horizontal and vertical directions, that contains the complete device being manufactured. [SEMATECH] Also called chip and microchip. Obsolete: bar, slice.

Die attach area n : the nominal area designated for die attaching to the package or leadframe. [SEMI G22-86] Contrast effective die attach area and die attach pad.

Die attach pad n : the nominal area designated for die attaching to the package or leadframe. Die attach pad is usually applied to leadframes. The term die attach area is usually applied to ceramic packages. [SEMATECH] Also see package and die.

Die attach surface n : in a ceramic semiconductor package, a dimensional outline designated for die attach. [SEMI G33-90] Also see package and die.

Die bonding (D/B) : an assembly technique that bonds the back side of an integrated circuit die to a substrate, header or leadframe. [SEMATECH]

Dielectric n 1 : a nonconductive material; an insulator. Examples are silicon dioxide and silicon nitride. [SEMATECH] 2 : a material applied to the surface of a ceramic or preformed plastic package to provide functions such as electrical insulation, passivation of underlying metallization, and limitations to solder flow. [SEMI G33-90]

Dielectric isolation (DI) n : a nonconductive barrier layer grown or deposited between two adjacent regions on a die to prevent electrical contact between the regions. [SEMATECH] Also see isolation.

Diffusion n : a high-temperature process in which desired chemicals (dopants) on a wafer are redistributed within the silicon to form a device component. [SEMATECH]

Dimple n : on a semiconductor wafer, a shallow depression in a wafer surface with a concave, spherical shape and gently sloping sides. NOTE – Dimples are macroscopic features that are visible to the unaided eye under proper lighting conditions. [ASTM F1241]

DIP : see dual inline package.

Dislocation n : a line imperfection in a crystal that either forms the boundary between slipped and nonslipped areas of a crystal or that is characterized by a closure failure of the

Burger's circuit. [ASTM F1241] Also called line defect. Also see slip.

Dopant n : in silicon technology, a chemical element incorporated in trace amounts in a semiconductor crystal or epitaxial layer to establish its conductivity type and resistivity. [Adapted from SEMI M9-90] Also see conductivity type, n-type, and p-type.

Dopant density n : in an uncompensated extrinsic semiconductor, the number of dopant impurity atoms per unit volume, usually given in atoms/cm^3, although the SI unit is atoms/m^3. Symbols: ND for donor impurities and NA for acceptor impurities. [ASTM F1241]

Doping n : the addition of impurities to a semiconductor to control the electrical resistivity. [SEMI M1-94 and ASTM F1241]

Drain n : one of the three major parts of a complementary metal oxide semiconductor transistor. [SEMATECH]

EBIC : See Electron Beam Induced Current.

Edge crown n : an increase of epitaxial layer thickness around the periphery of the wafer arising from differences in deposition rate. [SEMATECH]

EFM : See Electrostatic Force Microscopy

Electron Beam Induced Current (EBIC) : A failure analysis technique for electronic devices that displays the external current resulting from the electron hole pairs generated from the interaction of the electron beam and the PN junction. [ISTFA]

Electromagnetic Interference (EMI) n : any electrical signal in the non-ionizing (sub-optical) portion of the electromagnetic spectrum with the potential to cause an undesired response in electronic equipment. [SEMI E33-94]

Electrostatic discharge (ESD) n 1: a sudden electric current flow, such as between a human body and a metal oxide semiconductor, with potential damage to the component. [SEMATECH] 2 : the transfer of electrostatic charge between bodies at different electrostatic potentials. [SEMI E33-94]

Electrostatic force Microscopy (EFM) : A failure analysis tool that uses a repetitive single-pulse sampling approach to measure high frequency internal signals from ICs. [ISTFA]

Energy-dispersive X-ray spectrometer n : a detector used to determine which elements are present in a sample by analyzing X-ray fluorescence for energy levels that are characteristic of each element. [SEMATECH]

Epitaxial layer n : in semiconductor technology, a layer of a single crystal semiconducting material grown on a host substrate which determines its orientation. [SEMI M2-94 and ASTM F1241]

Epitaxy (epi) n : a silicon crystal layer grown on top of a silicon wafer that exhibits the same crystal structure orientation as the substrate wafer with a dissimilar doping type or concentration or both. Examples are p/p+, n/n+, n/p, and n/n. [SEMATECH] Also see epitaxial layer.

ESD : see electrostatic discharge.

Etch 1 n : a category of lithographic processes that remove material from selected areas of a die. Examples are nitride etches and oxide etches. [SEMATECH] 2 : in the manufacture of silicon wafers, a solution, a mixture of solutions, or a mixture of gases that attacks the surfaces of a film or substrate, removing material either selectively or nonselectively. [SEMI M1-94 and ASTM F1241] Also see anisotropic etch, preferential etch, dry plasma etch, reactive ion etch, and wet chemical etch.

Etchant n : an acid or base (in either liquid or gaseous state) used to remove unprotected areas of a wafer layer. Examples are potassium hydroxide, buffered oxide etch, and sulfur hexafluoride. [SEMATECH]

Etch pit n : a pit, resulting from preferential etching, localized on the surface of a wafer at a crystal defect or stressed region. [ASTM F1241]

Eutectic n : alloy or solution with components distributed in the proportions necessary to minimize the melting point. [SEMATECH] Also see azeotrope.

Excessive leakage n : in the testing of semiconductors, current that is above the specified limit for the particular test being conducted. [Sandia Labs]

Failure n : in failure analysis, an event where the semiconductor component does not function according to its intended use or specifications. [Sandia Labs]

Failure mechanism n : in failure analysis, a fundamental process or defect responsible for a failure. [SEMATECH]

Failure mode n : in failure analysis, the electrical symptoms by which a failure is observed to occur. Failure mode types include a catastrophic failure that is both sudden and complete and degraded failure that is gradual, partial, or both, as well as intermittent failures. [Sandia Labs]

Failure mode and effects analysis (FEMA) n : an analytically derived identification of the conceivable semiconductor failure modes and the potential adverse effects of those modes on the system and mission. [SEMATECH]

Failure pattern instance : a group of failing SRAM cells attributed to the same deforming event. [ISTFA]

Failure pattern type : A set of similar failure pattern instances. [ISTFA]

Fault n 1 : an accidental condition that causes a functional unit to fail to perform its required function. [SEMATECH] 2 : a defect causing out-of-spec operation of an integrated circuit. [SEMATECH] Also see exception condition and defect.

Fault coverage n : the percentage of a particular fault type that a test vector set will detect when applied to a chip. [1994 National Technology Roadmap for Semiconductors]

Fault dictionary n : a list of faults that a test vector will detect in a failing circuit, or a list of all such faults for each vector in a vector set. [1994 National Technology Roadmap for Semiconductors]

Fault model n : a model of the behavior of defective circuitry in an integrated circuit. Physical defects result in improper behavior in a circuit which must be modeled in order for test patterns to be a model, timing model, and bridging model. [1994 National Technology Roadmap for Semiconductors]

FET : see field-effect transistor.

FIB : see focused ion beam

Field-effect transistor (FET) n : a transistor consisting of a source, gate and drain, the action of which depends on the flow of majority carriers past the gate from the source to the drain. The flow is controlled by the transverse electric field under the gate. [SEMATECH]

Fishtails n : structures, attributed to substrate defects, either above or below the surface plane after epitaxial deposition; the "tails" are aligned in a particular crystallographic direction. [ASTM F1241] Also see crescents.

Fissure : see crack.

Flake n : material missing from one byt not the other side of a semiconductor wafer [SEMI M10-89]

Flake chip : see chip and peripheral chip.

Flaking : see peeling.

Flip-chip n : a leadless, monolithic structure that contains an integrated circuit designed to electrically and mechanically interconnect to a hybrid circuit. Connection is made to bump contacts covered with a conductive bonding agent on the face of the hybrid. [SEMATECH] Also called controlled collapse chip connect or C4

Fluorescence n : the emission of light as the result of, and only during, the absorption of radiation of shorter wavelengths. [IEEE]

Fluorescent Microthermographic Imaging (FMI) n : a failure analysis technique that uses a temperature dependent fluorescent compound and an optical pumping source to image temperature changes on a semiconductor device with near optical spatial resolution. [Sandia labs]

FMEA : see failure mode and effects analysis

FMI : see Fluorescent Microthermographic Imaging.

Focused ion beam (FIB) n : an imaging tool that can be used to deposit or etch materials on wafers. A focused ion beam is often used in the etch mode to selectively cleave structures for failure analysis. It is also used in photomask repair for removing or adding material, as necessary, to make the photomask defect free. [SEMATECH]

Fourier transform infrared spectroscopy: see Micro Fourier transform infrared spectroscopy.

FPI : see failure pattern instance.

FPT : see failure pattern type

Front end of line (FEOL) n 1: in semiconductor processing technology, all processes from wafer start through final contact window processing. [SEMATECH]

FTIR : see Micro Fourier transform infrared spectroscopy.

Functional pattern : see pattern, functional.

Functional probe n : the electronic testing of die on a wafer to determine conformance to specifications. [SEMATECH]

Functional test n : one or more tests to determine whether a circuit's logic behavior is correct. [1994 National Technology Roadmap for Semiconductors]

Galvanic corrosion: corrosion damage induced when two dissimilar metals coupled in a corrosive electrolyte. This can be seen in either wafer fab process or assembly process. [corrosiondoctor.org]

Gate n : an electrode that regulates the flow of current in a metal oxide semiconductor transistor. [SEMATECH]

Gate electrode n : the electrode of a metal oxide semiconductor field effect transistor (MOSFET); it controls the flow of electrical current between the source and the drain. [SEMATECH]

Gate oxide n : a thin, high –quality silicon dioxide film that separates the gate electrode of a metal oxide semiconductor transistor from the electrically conducting channel in the silicon. [SEMATECH]

Glass n : a deposited film of silicon dioxide with additives to adjust coefficient of thermal expansion, color, conductivity,

and melting point, generally doped with boron or phosphorous or both. [SEMATECH] Also see silicon dioxide.

Groove n : in a semiconductor wafer, a shallow scratch with rounded edges that is usually the remnant of a scratch not completely removed by polishing. [SEMI M1-94 and ASTM F1241]

Growth hillock : see pyramid.

Hermetic seal n : a coat applied in the final stage of thermal processing to seal the ceramic package and to protect the device from the external environment. [SEMATECH]

Hillock n : a defect caused by stress that raises portions of a metal (such as aluminum) film above the surface of the film. Localized stress within the metal film may elevate portions of the film through the adjacent dielectric layer, resulting in a metal extrusion and a short to the next metal layer. [SEMATECH] Also see pyramid.

Hole n 1 : of a semiconductor, a mobile vacancy in the electronic valence structure that acts like a positive electron charge with a positive electron charge with positive mass; the majority carrier in p-type. [SEMI M1-94 and ASTM F1241] 2 : in plastic and metal wafer carriers, the area through which a pin from another wafer carrier can enter for the transfer of wafers. [SEMI E1-86] Also see wafer carrier.

Hot carriers n : those carriers, which may be either electrons or holes that have been accelerated by the large traverse electric field between the source and the drain regions of a metal oxide semiconductor field - effect transistor (MOSFET). They can jeopardize the reliability of a semiconductor device when these carriers are scattered (that is, deflected) by phonons, ionized donors or acceptors, or other carriers. The scattering phenomenon can manifest itself as substrate current, gate current, or trapped charges. [SEMATECH] Also see trapped charges.

IC : see integrated circuit.

IDDQ : abbreviation for direct drain quiescent current. See static current test.

Impact test n : in component testing, a test performed to determine particle contribution as a result of mechanical shock to the component. [SEMATECH] Also called particle impact noise detection or PIND

Implant : see ion implantation.

Impurity n : a chemical or element added to silicon to change the electrical properties of the material. [SEMATECH] Also see dopant, ion implantation.

Inclusion n : discrete second phases (oxides, sulfides, carbides, intermetallic compounds) that are distributed in a metal matrix. [SEMATECH]

Indent n : on a semiconductor wafer, an edge defect that extends from the front surface to the back surface. [ASTM F1241] Contrast chip.

Insulator n : a substance that will not conduct electricity; for example, silicon dioxide and silicon nitride. [SEMATECH] Contrast conductor.

Integrated circuit (IC) n 1: two or more interconnected circuit elements on a single die. [SEMATECH] 2 : a fabrication technology that combines most of the components of a circuit on a single-crystal silicon wafer. [SEMI Materials, Vol. 3, Definitions for Semiconductor Materials]

Interference contrast microscope n : an optical microscope that reveals surface details of an object in which there is no appreciable absorption by using the interference between two beams of light. [Adapted from ASTM F1241] Also called Nomarski Interference Contrast

Interlevel dielectric n : an insulating film between two conductive film layers, as between poly and aluminum or between layers of aluminum. [SEMATECH]

Interstitial n : in a crystalline solid, an atom that is not located on a lattice site. [SEMATECH]

Intrinsic semiconductor n : a semiconductor in which the density of electrons and holes is approximately equal . [SEMATECH] Contrast extrinsic semiconductor

Ion implantation (I 2 , II) n : a high-energy process that injects an ionized species such as boron, phosphorus, arsenic, or other ions into a semiconductor substrate. [SEMATECH]

I/O pins n : connections to an integrated circuit through which input and/or output (I/O) signals pass. [1994 National Technology Roadmap for Semiconductors]

Isolation n : an electrical separation of regions of silicon on a wafer; for example, boron diffusion to isolate a transistor. [SEMATECH] Also see dielectric isolation.

Junction spiking n : the penetration of a junction by aluminum, which occurs when silicon near the junction dissolves in aluminum and migrates along the interconnect lines. Aluminum then replaces silicon at the junction. [SEMATECH]

Kirkendall void n : voids induced in a diffusion couple between two metals that have different interdiffusion coefficients. [SEMATECH]

Large scale integration (LSI) n : the placement of between 100 and 1000active devices on a single die. [SEMATECH]

Laser-scattering light event n: a signal pulse that exceeds a preset threshold, generated by the interaction of a laser beam

with a localized light scatterer (LLS) at a wafer surface as sensed by a detector. [ASTM F1241]

Laser Voltage Probe (LVP) : a technique that measures the photons absorbed within a junction area. [ISTFA]

Layout n 1 : the physical geometry of a circuit or die. [1994 National Technology Roadmap for Semiconductors] 2 : the process of creating the physical geometry of a circuit or die. [1994 National Technology Roadmap for Semiconductors] 3 : see composite drawing.

LDD : see lightly doped drain.

Life test n : in semiconductor reliability, a test designed to operate the semiconductor until it fails by elevating both temperature and voltage to accelerate the aging process. [Sandia Labs]

Lightly doped drain (LDD) n : a metal-oxide semiconductor (MOS) device design in which the drain doping is reduced to improve breakdown voltage. [SEMATECH]

Line defect : see dislocation.

Liquid-metal embrittlement: The brittle failure of a normally ductile metal when in the presence of a liquid metal and subsequently stressed in tension. [ISTFA]

Light Induced Voltage Alteration (LIVA): An advanced failure analysis technique that utilizes a laser scanning microscope and various electronics to produce localized photons within the semiconductor device circuitry. [ISTFA]

LSI : see large scale integration.

LVP : see laser voltage probe.

Metallization void n : the absence of a clad, evaporated, plated or screen printed metal layer or braze from a designated area. [SEMI G58-94] Also called metal void.

Metal void : see metallization void.

MFM-CCI : see magnetic current imaging.

Microchip : see die.

Micro Fourier transform infrared spectroscopy (FTIR) : a technique, considered to be non-destructive, based on infrared photon absorbtion typically used to determine polymers, plastics, fibers, and organic films with an approximate sensitivity of 1 - 10 ppm with a resolution down to ~15 μm. Also called Fourier transform infrared spectroscopy.

Miller Indices : a numeric convention that describes the orientation of the atomic planes in a crystal lattice, i.e., the crystal faces, of a crystalline material. Also called crystal indices. Also see crystallographic notation.

Moon crater n : on a semiconductor wafer, surface texture that results when a wafer floats during the initial stages of chemical polishing in a rotating cup etcher. [ASTM F1241]

Motorboat : see comet.

Mottled adj : pertaining to the existence on a wafer of a of material in a window that prevents the window from being properly opened. [SEMATECH]

Mound n : on a semiconductor wafer, an irregularly shaped projection on a semiconductor wafer surface with one or more irregularly developed facets. [ASTM F1241] Contrast pyramid. Also called mouse bite.

Nano hardness tester (NHT): a technique that places a weighted top on the film surface and measures the maximum load that can be applied without deforming the film. [ISTFA]

Nick : see chip

NHT : see Nano hardness tester

Notch n 1: an unexpected intrusion or reduction of line width in patterned geometries. May also be a V-shaped intrusion into the perimeter of a wafer. The intrusion is used to align the wafer during process. [SEMATECH] 2 : on a semiconductor wafer, an intentionally fabricated indent of specified shape and dimensions oriented such that the diameter passing through the center of the notch is parallel with a specified low index crystal direction. [SEMI M1-94 and STM F1241]

Oil canning n : in metal lid/perform assembly, lid concavity after sealing. [SEMI G53-92]

Optical Beam Induced Resistance CHange (OBIRCH): An advanced failure analysis technique that uses a laser scanning microscope to detect a change in the current under constant voltage conditions. [ISTFA]

Overcoat : see passivation

Oxide defect n : an area of missing oxide on the back surface of back-sealed wafers discernible to the unaided eye. [ASTM F1241]

Oxide etch n : an etch process in which unprotected areas of the oxide layer are eroded by use of a chemical to expose the underlying layer. [SEMATECH]

Parametric test n : wafer-level testing of discrete devices such as transistors and resistors. [SEMATECH]

Parasitics n : unwanted circuit components (for example, capacitors or resistors) present in a design. [1994 National Technology Roadmap for Semiconductors]

Particle n 1: a minute quantity of solid or liquid matter. [SEMATECH] Also called dirt. 2 : in the manufacture of photolithographic pellicles, material that can be distinguished from the film, whether on the film surface or embedded in the film. [SEMI P5-94] 3 : the re-plating step in which a catalytic material, often a palladium or gold compound, is absorbed on a surface to act as sites for initial stages of deposition. [ASTM B374-93]

Particulate 1 n: discrete particles of dirt or other material. [ASTM F1241] Also see dirt. 2 n (dust) : discrete particle of material that can usually be removed by (nonetching) cleaning. [SEMI M10-89] 3 adj : describes material in small, discrete pieces; anything that is not a fiber and has an aspect ratio of less than 3 to 1. Examples are dusts, fumes, smokes, mists, and fogs. [SEMATECH]

Particulate contamination n : on a semiconductor wafer, a particle or particles on the surface of the wafer. [ASTM F1241]

Passivation n : deposition of a scratch-resistant material, such as silicon nitride and/or silicon dioxide, to prevent deterioration of electronic properties caused by water, ions, and other external contaminants. The final deposition layer in processing. [SEMATECH] Also called overcoat and cap deposition.

Peeling n: any separation of a plated, vacuum deposited, or clad metal layer from the base metal of a leadframe, lead, pin, heat sink or seal ring from an under plate, or from a refractory metal on a ceramic package. Peeling exposes the underlying material. [SEMI G61-94] Also called flaking. Contrast blister metal.

Peripheral chip n 1 : crystallographic damage along the circumference formed in the periphery of the specimen through conchoidal fracture and resultant spalling. [ASTM F1241] Also called flake chip or surface chip.

Picosecond Imaging Circuit Analysis (PICA): A technique that measures time-dependent hot carrier induced light emission from the integrated circuit (IC) both spatially and temporally, thus enabling failure analysis and timing evaluation of a device. [ISTFA]

Pinhole n 1 : minute defect or void in a film, mask , or resist, usually the result of contaminants. [SEMATECH] 2 : a small opening that extends through a covering, such as a resist coating or an oxide layer on a wafer. [SEMI P2-86]

Pit n 1 : in a wafer surface, a depression in a wafer surface that has steeply sloped sides which meet the surface in a distinguishable manner, in contrast to the rounded sides of a dimple. [ASTM F1241] Also see slip and dislocations. 2 : in semiconductor packages, plastic or ceramic, or in the lead-frames, a shallow depression or crater. The bottom of the depression must be visible in order for the term to apply. A pit is formed during the component manufacture. [SEMI G61-94] Contrast chip. 3 : in flat panel display substrates, a small indentation on the glass substrate surface. [SEMI D9-94]

Point defect n : a localized crystal defect such as a lattice vacancy, interstitial atom, or substitutional impurity. [ASTM F1241] Contrast with localized light scatter,

Poly : see polycrystalline silicon.

Polycrystalline adj : describes a form of semiconductor material made up of randomly oriented crystallites and containing large angle grain boundaries, twin boundaries, or both. [SEMI M10-89 and ASTM F1241] Contrast single crystal. Also see amorphous silicon.

Polycrystalline silicon (poly) n 1 : a nonporous form of silicon made up of randomly oriented crystallites or domains, including glassy or amorphous silicon layers. [ASTM F399-88] Also called poly and poly silicon. Contrast amorphous silicon and single crystal.

Polysilicon: see polycrystalline silicon.

Precipitate n 1 : within a silicon lattice, a region of silicon oxide frequently manifested as an etch pit. [ASTM F1241] Also see crystal lattice and pit. 2 : in a gallium arsenide wafer, a localized concentration of dopant that is insoluble. Precipitate is formed during crystal growth and during any process in which the temperature is sufficient to provide the necessary impurity mobility. [SEMI M10-89]

Process-induced defect (PID) n : defect(s) added to the wafer as a result of a processing step. The PID wafer undergoes the same process sequence as a product wafer. PID wafer data is a closer approximation of actual process defect contributions than particles per wafer pass (PWP) wafer data. [SEMATECH]

Pyramid n : a structure displaying [111] facets that appears on surfaces after epitaxial growth. DISCUSSION – a pyramid originates at the interface of the substrate and the epi layer and is due to various imperfections at the beginning of epi growth. [ASTM F1241] Also called growth hillock. Also see hillock and mount.

Quiescent Signal Analysis (QSA) : an electrical test based diagnostic technique that uses I_{DDQ} measurements made at multiple chip supply pads as a means of locating shorting defects in the layout. [ISTFA]

QSA : see quiescent signal analysis.

Reactive Ion Etching (RIE) n : a dry-etch process using electrical discharge to ionize and induce ion bombardment of the wafer surface to obtain the required etch properties. [SEMATECH]

Registration n 1 : the accuracy of the relative position of all functional patterns on any reticle with the corresponding

patterns of any other reticle of a given device series when the reticles are properly superimposed. [ASTM F127-84] 2 : a vector quantity defined at every point on the wafer. It is the difference, R, between the vector position, P1, of a substrate geometry and the vector position of the corresponding point, P0, in reference grid. [SEMATECH] 3 : in the overlay capabilities of wafer steppers, a vector quantity defined at every point on the wafer. It is the difference, R, between the vector position, P1, of a substrate geometry, and the vector position of the corresponding point, P0, in a reference grid. [SEMI P18-92]

Residue n : any undesirable material that remains on a substrate after any process step. [ASTM F127-84 and SEMI P3-90]

Resistive Interconnection Localization (RIL): a scanning laser microscope analysis technique that directly and rapidly localizes defective vias, contacts, and conductors from the front side and backside. [ISTFA]

RIE : See Reactive Ion Etching

RIL : See resistive interconnection localization

Root cause n 1 : in failure analysis, the fundamental incident or condition that initially caused the failure to occur. [Sandia Lab]

SAM : see Auger electron spectroscopy

Saucer pits : see shallow etch pits.

Saw-blade defect n 1 : on semiconductor wafers, a roughened area visible after polishing with a pattern characteristic of the saw blade travel. [STM F1241] Also see saw marks. 2 : a depression in the wafer surface made by the blade, which may not be visible before polishing. [SEMI M10-89]

Saw exit chip n : in gallium arsenide technology, an edge fragment on a wafer broken off at the point at which the saw completed its cut the wafer. A saw exit chip is typically straight or arc shaped, not irregular, and sometimes can be confused with the orientation flats. [SEMI M10-89] Contrast saw exit mark.

Saw exit mark n : in silicon technology, a ragged edge at the periphery of a wafer consisting of numerous adjacent small adjoining edge chips resulting from saw blade exit. [ASTM F1241] Also see saw marks, saw exit chip.

Saw-kerf : see scribe line

Saw marks n : on a wafer, surface irregularities in the form of a series of alternating ridges and depressions in arcs, the radii of which are the same as those of the saw blade used for slicing [ASTM F1241] Also see saw exit mark.

Scanning Auger microprobe (SAM) : see Auger electron spectroscopy

Scanning electron microscope (SEM) n : a device that displays an electronically scanned image of a die or wafer for examination on a screen or for transfer onto photographic film; displays a higher magnification than an optical microscope. [SEMATECH]

Scanning Probe Microscopy (SPM) : Provides topographic imaging coupled with a variety of material characterization information such as thermal magnetic, electric, capacitance, resistance and current with nano-meter scale resolution. [ISTFA]

Scanning Thermal Microscope (SThM) : A failure analysis technique for electronic devices that uses a resistive probe to detect temperature distribution with an accuracy of 5mK and a local resolution of 50 nm. [ISTFA]

Scanning tunneling microscope (STM) n : an instrument for producing surface images with atomic scale lateral resolution, in which a fine probe tip is raster scanned over the surface and the resulting tunneling current is monitored. [SEMATECH]

Scratch n : on semiconductor wafers, a shallow groove or cut below the established plane of the surface, with a length to width ratio greater than 5:1 [ASTM F1241] Also see macroscratch, microscratch.

Scum n : resist residue located in a window or along the foot of patterned geometry. [SEMATECH]

Secondary Ion Mass Spectrometry (SIMS) n : an analytical tool that uses a focused ion beam that is directed to a solid surface, removing material in the form of neutral and ionized atoms and molecules. The secondary ions are then accelerated into a mass spectrometer and separated according to their mass-to-charge ratio. [Center for Microanalysis of Materials]

Seebeck Effect Imaging (SEI) n : An advanced failure analysis technique that utilizes infrared laser to isolate a defect within a die by thermally altering the defect's electrical characteristic without biasing the device. [ISTFA]

SEM : see scanning electron microscope.

Semiconductor n : an element that has an electrical resistivity in the range between conductors (such as aluminum) and insulators (such as silicon dioxide). Integrated circuits are typically fabricated in semiconductor materials such as silicon, germanium, or gallium arsenide. [SEMATECH]

Shallow etch pits n : on a wafer etch pits that are small and shallow in depth under high magnification greater than 200X [ASTM F1241] Also called saucer pits. Also see haze

Short : see bridge

Silicon (Si) : a brownish crystalline semimetal used to make the majority of semiconductor wafers. [SEMATECH]

Silicon dioxide (SiO_2) n : a passivation layer thermally grown or deposited on wafers. It is resistant to high temperatures. Oxygen or water vapor is used to grow silicon dioxide at temperatures above 900°C. Silicon dioxide is used as a masking layer as well as an insulator. [SEMATECH] Also called quartz. Also see glass.

Silicon nitride (Si_3N_4) (abbr. SiN) n : a passivation layer chemically deposited on a wafer at temperature of between 600°C and 900 °C to protect the wafer from contamination . Silicon nitride is also used as a masking layer and as an insulator. [SEMATECH]

Silicon on insulator (SOI) n : a novel substrate for high-performance, low-power, and radiation-hard CMOS applications that offers process simplification, improved scalability, latch-up free and soft-error free operation, improved sub threshold slope, and drastic reduction in parasitic capacitance. At this writing, there are two manufacturing-oriented techniques to build SOI : SIMOX and bonded. [SEMATECH].

SIMS : see Secondary Ion Mass Spectrometry

Slice : see wafer.

Slip n : in semiconductor wafers, a process of plastic deformation in which one part of a crystal undergoes a shear displacement relative to another in a manner that preserves the crystallinity of each part of the material. DISCUSSION – After preferential etching,, slip lines are evidenced by a pattern of one or more parallel straight lines of dislocation etch pits that do not necessarily touch each other. On [111] surface, group of lines are incline at 60° to each other; on [100] surfaces, they are inclined at 90° to each other. [SEMI M10-89 and STM F1241] Also see pit.

Slip line n : a step occurring at the intersection of a slip plane with the surface. [ASTM F1241]

Slip plane n : the crystallographic plane on which the dislocations forming the slip move. [ASTM F1241]

Small scale integration (SSI) n : the placement of between 2 and 10 active devices on a single die. [SEMATECH] Also see die.

Smudge n : dense local area of contamination usually caused by handling or fingerprints. [SEMI M1-94 and ASTM F1241] Also see dirt.

Snowball n : on a semiconductor wafer, a track with the appearance under magnification of a snowball rolled through snow. [ASTM F1241]

Soft defect localization : A laser scanning failure analysis methodology that combines localized heating and detection of changes in the pass/fail probability of a vector set. [ISTFA]

SOI : see silicon on insulator.

SOS : see silicon on sapphire.

Source n : one of the three major components of a CMOS transistor. [SEMATECH]

Spike n 1 : in a epitaxial wafer surface, a tall, thin dendrite or crystalline filament that often occurs at the center or recess. [ASTM F1241] 2 : an extreme structure that has a large ratio of height-to-base width and no apparent relation to epitaxial film thickness. [SEMATECH] Also see pyramid and mound.

SPM : see scanning probe microscopy.

SPP : See statistical post processing.

SQUID (Super-conducting quantum interference device) microscope n. : A tool that uses a highly sensitive magnetic field that works at cryogenic temperatures (90 K) to detect magnetic field position which is then be Fourier transformed to produce current density maps based on Biot-Savart law. [ISTFA]

SSI : see small scale integration.

Stacking fault n : in a crystal, a two-dimensional defect caused by a deviation from the normal stacking sequence of atoms. [ASTM F1241]

Stain n 1 : a solution applied to a cross-sectioned silicon device to reveal the location of various structures. [SEMATECH] 2 : contaminant in the form of streaks that are chemical in nature and cannot be removed except through further lapping or polishing. Examples are “white” stains that are seen after chemical etching as white or brown streaks. [SEMI Materials, Vol. 3, Definitions for Semiconductor Materials] 3 : a two-dimensional, contaminating foreign substance on a component surface. [SEMATECH] Also see contamination and foreign material. 4 : in flat panel display substrates, any erosion of the surface; generally cloudy in appearance, it sometimes exhibits apparent color. [SEMI D9-94] 5 : area contamination that is chemical in nature and cannot be removed except through further lapping or polishing [ASTM F1241]

Step coverage n : the ratio of thickness of film along the walls of a step to the thickness of the film at the bottom of a step. Good step coverage reduces electromigration and high resistance pathways. [SEMATECH]

Statistical post processing (SPP) : a statistical technique that separates the effects of defects from normal wafer-to-wafer variation. [ISTFA]

STM : see scanning tunneling microscope.

SThM : see scanning thermal microscope.

Stuck-at fault n : a fault in a manufactured circuit causing an electrical node to be stuck at a logical value of 1 or a logic value of 0, independent of the input to the circuit. [1994 National Technology Roadmap for Semiconductors]

Substrate n : in the manufacture of semiconductors, a wafer that is the basis for subsequent processing operations in the fabrication of semiconductor devices or circuit. [ASTM F1241]

Surface chip : see peripheral chip

Surface defects n 1 : in the manufacture of silicon on sapphire (SOS) epitaxial silicon wafers, mechanical imperfections, SIO_2 residual dust, and other imperfections visible on the wafer surface. Some examples of surface defects are: dimple, pits, particulates, spots, scratches, smears, hillocks, and polycrystalline regions. [SEMI M4-88] 2 : in flat panel display substrates, a marking, tearing or single line abrasion on the glass surface. [SEMI D9-94]

TCR : See Thermal coefficient of resistance

TDR : See Time domain reflectometry

Tester pattern generation (TPG) n : the generation of a program that runs on an integrated circuit hardware tester (integrated circuit tester). The purpose of this program is to permit test vectors to be applied to determine the performance of the integrated circuit. [1994 National Technology Roadmap for Semiconductors] Also called tester program generation.

Test pattern : see pattern, test.

Test techniques n : any methods used for the expressed purpose of testing integrated circuits. Examples include build-in self test (BIST), automatic test pattern generator (ATPG), static current test (IDDQ), and boundary scan. [1994 National Technology Roadmap for Semiconductors]

Test vectors n : sequences of signals applied to the pins of an integrated circuit to determine whether the integrated circuit is performing as it was designed. [1994 National Technology Roadmap for Semiconductors]

Thermal coefficient of resistance (TCR): A fundamental characteristic of metallization and is dependent only on the residual resistivity of the metal which is determined by differences in the structural order of a pure, bulk metal, that contribute to electron scattering. [ISTFA]

Time Domain Reflectometry (TDR): Analysis technique that uses a low voltage, low current, and very short rise time voltage pulse to determine the impedance of a signal trace as a function of time. [ISTFA]

Tin whiskers : hair-like growths of near-perfect single crystalline structures of tin that grow from some electroplated tin surfaces. [ISTFA]

Thermal Induced Voltage Alteration (TIVA) : An advanced failure analysis technique that uses a laser scanning microscope to locally heat a region to stimulate an alteration in the voltage under constant current conditions. [ISTFA]

Total reflection X-ray fluorescence (TXRF) n : an analytical method usually used to characterize the level of metallic (and non-metallic element) surface contamination. IN TXRF, an X-ray beam excites fluorescence from the contamination that is present on a silicon surface. Since the beam is incident at grazing angles, it totally reflects from the surface, thus maximizing the signal. [SEMATECH]

Trapped charges n : charges trapped either in the gate oxide or, in the case of a lightly doped drain (LDD) metal-oxide semiconductor field-effect transistor (MOSFET), in the spacer region. Trapped charges in the gate or the spacer lead to threshold voltage shift or to transconductance degradation, respectively. [SEMATECH]

TXRF : see total reflection X-ray fluorescence.

Undercutting n : the lateral etching into a substrate under a resistant coating, as at the edge of a resist image. [ASTM F127-84]

Unencapsulated thermal test chip n : an unpackaged, specially designed silicon die with standard test junctions that, after mounting into a package, may be used to thermally characterize that package. This technique is useful in determining the difference between various vendors' packages and package designs. [SEMATECH]

Via n : a connection between two conducting layers above the silicon surface that is created by a different material or deposition step [Sandia Lab]

Void 1 : see dielectric void. 2 : see glass void. 3 : see metallization void.

Wafer n : in semiconductor technology, a thin slice with parallel faces cut from a semiconductor crystal. [ASTM F1241] Also called a slice. Also see substrate.

Well n : a localized n-type region on a p-type wafer or a p-type region on a n-type wafer. [SEMATECH]

X-ray fluorescence n 1 : the property of atoms to absorb X rays and emit light of characteristic wavelengths. [SEMATECH] 2 : a material diagnostic technique that determines the surface concentration of contaminants. [SEMATECH]

X-ray laminography : a radiographic 3-D technology that provides a focused image slice at a selected plane and analyzes the images using a set of algorithms. [ISTFA]

XRL : see X-ray laminography